UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO, LTD; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR INC., Defendants.	Case No. 2:22-cv-293-JRG JURY TRIAL DEMANDED (Lead Case)
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

PLAINTIFF NETLIST INC.'S REPLY CLAIM CONSTRUCTION BRIEF

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I. The "rank" terms

A. Netlist did not waive its construction.

Netlist made clear at the outset that a "rank" requires multiple devices. Dkt. 94-1 (Netlist's P.R. 4-3s) at 2. The refinements in Netlist's opening brief are nothing like the *Lodsys* case. There, a party proposed a new construction after the close of claim construction briefing and shortly before the *Markman*. *Lodsys, LLC v. Brother Int'l Corp.*, 2013 WL 2949959, at *19 (E.D. Tex. June 14, 2013). Here, Defendants had ample opportunity to address Netlist's constructions in their responsive brief.

B. A "rank" of "DDR memory devices" requires multiple memory devices.

Schering Corp. v. Amgen Inc. held that the court "must determine what the term meant at the time the patentee filed the . . . application." 222 F.3d 1347, 1353 (Fed. Cir. 2000). Micron conceded that a POSITA would believe the asserted patents "were supposed to comply with JEDEC standards." Ex. 4, 38:11-19; Ex. 5, ¶ 44. The '912 claims require "DDR" memory devices. DDR memory devices are standardized. Op. Br. 1-2. JEDEC standards require that a rank in the context of DDR memory devices include more than one DDR memory device. Micron's 30(b)(6) representative on technical issues confirmed that a DDR "rank" requires two or more memory devices:

> Q. And in JEDEC DDR parlance, a rank is two or more memory devices. Is that correct?
> A. A rank is defined as a group that comprises a full 64-bit data bus. So it would be, at a minimum, the number of devices that are required to meet that full data bus.
> Q. And, historically, how many has that been?
> A. So for a x8-based module, that would be ***eight devices***. For a x4-based, so four DQs in a DRAM -- x8 is going to be 8 DQs. So four DQs, x4 configuration, that would be ***16 DRAM***.

Ex. 33, 51:9-19; 10:17-21 (witness is the most senior engineer at Micron in module development).

Patents do not include, and preferably omit, that which is known in the art. *Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 982 (Fed. Cir. 2021). By discussing ranks of DDR memory devices, the patent is necessarily defining ranks as multiple devices, because DDR ranks must have multiple devices to operate. Accordingly, Dr. Stone admitted that "[a] POSA would believe that these [asserted] patents were supposed to comply with JEDEC standards," Ex. 4, 38:2-39:8, and that "[i]n the present

and past for this definition of a rank . . . it has been more than one chip." Ex. 4, 44:15-20.[1] Defendants assert that Dr. Stone was not "asked to opine on" the meaning of "rank," Resp. Br. 5, but they do not challenge his expertise as POSITA, nor do they claim the term was specially defined in the '912 patent.

The intrinsic record is of no assistance to Defendants.

- Contrary to Defendants' assertion, the claim language in the '215 patent does not define the number of devices in a rank; it defines one of the devices in the rank and specifies what it must do. Op. Br. 11-12. And this is irrelevant to the '912 patent, which has a different specification.

- The '912 patent claims recite "DDR" memory devices, such as claim 15:

> a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices ***having a first number of DDR memory devices arranged in a first number of ranks***;

This language recites a module that has multiple "DDR memory devices" (as opposed to some other type of memory device) ("a plurality"), thereby defining the type of devices, and then states the module has multiple "ranks" containing "DDR memory devices" (as opposed to some other type of memory device): "first number of DDR memory device**s**" (plural) in each of the rank**s** (plural). That a rank in the context of DDR devices has multiple devices does not make "a plurality of double-data rate (DDR memory)" devices superfluous, because this language is used to define the class of memory device.

- Defendants point to claim 55 of the '912 patent, which recites the following limitation:

> and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages ***having a total bit width equal to the summed bit widths DDR DRAM chip packages of the rank***, ... Ex. 1 ('912), p. 46, 5:56-59.

The purpose of this language is not to narrow "rank" to a "rank" with multiple devices; it is to define the combined bit-width of the chips in the rank.

[1] Contrary to Defendants' argument, Resp. Br. 7-8, Netlist does not propose limiting the term "DDR memory devices" to products compliant with all aspects of JEDEC standards at the time of the '912 patent. Netlist explained why a POSITA would understand the term "rank" in the context of DDR devices as requiring more than one memory device per rank . Op. Br. 2-3.

- Defendants cite to 24:13-24 and Fig. 6A of the '912 patent, but neither mention "rank":

> FIG. 6A schematically illustrates a circuit diagram of a conventional memory module 100 showing the interconnections between the DQ data signal lines 102 of the memory devices "a" and "b" ***(not shown)*** and their DQS data strobe signal lines 104. In certain embodiments the electrical signal lines are etched on the printed circuit board. As shown in FIG. 6A, each of the memory devices has their DQ data signal lines 102 electrically coupled to a common DQ line 112 and the DQS data strobe signal lines 104 electrically coupled to a common DQS line 114.

Id., 24:13-24. That the memory devices are "not shown" in Fig. 6A confirms that this disclosure has nothing to do with defining the number of "ranks" in a "conventional memory module." Memory devices "a" can be a plurality of memory devices and memory devices "b" can be a separate plurality.

- Defendants' reliance on the embodiment in logical State 4 of Table 1 is misplaced. Resp. Br. 3 (citing Ex. 1, 8:48-64; Ex. 2, 16:66-17:13; Ex. 3, 19:14-27). Defendants argue that the reference to plural "memory devices 30" in Table 1 refers to the two memory devices in separate ranks, but do not dispute that "memory devices 30" are consistently described in the specification as part of multi-device ranks. Op. Br. 5. And as explained in the Opening Brief, the PTAB interpreted this embodiment in light of an incomplete record. *Id.* at 6.

- The specification's description of both 32-bit memory modules and 32-bit memory devices does not suggest a POSITA would use a single 32-bit device for a 32-bit module. Resp. Br. 3. The '912 claims are limited to "DDR memory devices." There are no 32-bit DDR memory devices, and there were not any at the time of the '912 patent filing. Exs. 7, 8 (DDR and DDR2 standards specifying x4, x8, and x16 device widths); Ex. 34 at 15 (specifying "x4, x8, and x16 DDR3 SDRAM devices"); Ex. 35 at 9 (specifying "x4, x8, and x16 DDR4 SDRAM devices"); Ex. 36, at 33 (specifying "x4, x8, and x16 DDR5 SDRAM devices."). A POSITA would read the specification with this in mind.

- The citation of Lee is a *non-sequitor*. Resp. Br. 3. The Lee patent is irrelevant to the '912 patent, as the examiner never discussed the reference, and Lee does not deal with DDR memory devices as required by the claims of the '912 patent.

- Defendants contend that neither the Central Reexamination Unit (CRU) nor the Board construed the term "rank" in rejecting Requesters' theory that Amidi taught transmitting a command signal to "only one DDR memory device at a time" of '912 claim 16. Resp. Br. 4. Defendants first cite Paragraph 54 of the CRU decision, which does not state that Amidi discloses multiple devices in a rank. Instead, it states that the claims require multiple devices in a rank with only one responding:

> The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank. Ex. 10 at 3866.

Likewise, page 76 of the Board's decision observes that it would not be obvious to send a command signal to one device in a multi-device rank:

> Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank. Ex. 11 at 76.

This would only support the affirmance of the claims if they required a rank with multiple devices.

- While the PTAB's preliminary construction in the pending IPRs is not consistent with Netlist's proposal—or the previous determination of the CRU on re-examination as affirmed by the Board and Federal Circuit—that IPR tentative construction lacked the benefit of Dr. Stone's and Mr. Holbrook's admissions. *See* Op. Br. 6-7. Defendants now assert that "Jacob eliminates any ambiguity" by stating that ranks can include "as few as one device per rank." Resp. Br. 5. But Defendants fail to note the context of that quote, which describes "embedded systems that do not require as much capacity or data bus width" and contrasts those systems with "modern memory systems." Ex. 18, 414. The patent is directed to memory modules, not embedded systems. Ex. 1 ('912), p. 23, 1:20-24 ("Field of Invention[:] The present invention relates generally to memory modules of a computer system . . . .").

C. The '417 and '215 patents also preclude single-device ranks.

While the '215 and '417 patents do not share an identical disclosure or express claim recitation

of "DDR memory devices" with the '912 patent, Micron's expert admitted that they too require JEDEC-compliant memory modules. Ex. 4, 38:2-39:8; Ex. 5, ¶ 44.

D. A "rank" of memory devices corresponds to a predetermined group of memory devices and a fixed bit-width.

Defendants contend that the patents contemplate dynamically reconstituting physical memory devices into ranks of varying bit widths, Resp. Br. 6-7, but the patents suggest no such thing. Op. Br. 7-8 (explaining how, in the context of the '912 patent, each "rank" of DDR memory devices is depicted as mounted on a PCB and associated with a unique chip-select signal). The JEDEC standards comport with this understanding of a fixed width, as confirmed by Micron's expert. Ex. 4, 48:1-3; Ex. 9 at 5; Ex. 19 at 6. Defendants identify only one disclosure allegedly supporting their position, which plainly relates to manufacturing a module with a different capacity, not adding or reconfiguring memory devices on the fly. Ex. 1, 2:24-31 (describing increasing the "number of memory devices of a memory module" by increasing the number of devices per rank or the number of ranks).

E. The inventions can "send or receive" less than the full module bit-width.

Nothing in the patents requires that all the memory devices in one rank simultaneously send or receive data under all circumstances. *See* Op. Br. 9-10. Indeed, claim 16 of the '912 patent claims a memory module "where the command signal is transmitted to only one DDR memory device at a time." Ex. B, 3:9-43. Defendants cite the Jacob treatise reference to "DRAM devices that operate in lockstep," but that extrinsic evidence cannot override the express teachings of the patents, particularly when one of Samsung's own experts agreed with Netlist's position that a "rank" may have the capability to partially output the full bit-width of the module. *See* Op. Br. 9; Ex. 31, 36:2-10, 37:8-14. Defendants also allege that Netlist itself argued that a rank's devices must "operate in lockstep," Resp. Br. 7, but the cited IPR briefs merely describe the Jacob treatise. Ex. G, 34; Ex. Y, 12-14.

II. <u>The "signal" terms do not encompass packetized control and address information</u>

Packetized information transfer is not an electrical impulse, i.e., a high or low which translates

into a 1 or 0, but is instead a group of 1s and 0s linked together. The intrinsic record makes no reference to packetized transfer of information as being the same as signals. The plain meaning also recognizes this distinction. Micron's senior module designer testified that there is a distinction between signals and packets. Ex. 33 at 52:13-18 ("Q. What's the difference between a signal and an encoded packet of data? A. So a signal, from my understanding, is a single, defined signal, a 1 or a 0. Encoded data, group of data, would be a group of 1s and 0s that would be encoded by a device.").

III. Netlist amended claims to recite "in response"; no additional construction is proper

There is no basis to re-write the claim and replace the term "in response" to with "use." The claims were amended to precisely recite "in response at least in part to [four signals]" with "and" after each signal. No more additional construction is necessary. In reexamination, Netlist stated:

> [T]he amended claims now also require that the logic element generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. ***Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals***. Instead, the control signals (rcs0a, rcs0b, rcsla, rcslb, rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select signals. . . . Defs. Ex. P at 52.

The distinction was that all recited signals must be received, not that all four signals will be sent on to the memory device or will be combined in some type of hash by Amidi's CPLD to create the signal sent on to the memory device. Likewise, in briefing before the Federal Circuit Netlist stated:

> Netlist distinguished its amended claims over prior art that failed to disclose or suggest a ***logic element responding to all four enumerated signals***. Defs. Ex. Q at 12.
>
> In adopting that construction, the Board repeatedly cited the amended claims' plain language: "as now claimed, claim 1 recites the logic element 'generates chip-select signals' in response to signals (i)-(iv)." . . . . It explained that the prior art references "collectively do not teach or suggest sufficiently to one skilled in the art the 'logic element' limitation generating CAS signals ***in response to*** both a row address signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv)." Defs. Ex. Q at 24 (internal citations omitted).

In other words, the issue in the reexamination was that the prior art did not receive all four signals and therefore could not act after receiving all four signals. But that is not what Defendants mean by

"use." It appears that at a later stage Defendants will require that "use" means that all four signals are sent to the memory device, or that all four signals are combined together via the translation logic equation to generate the signal that is sent to the memory device, contrary to certain the embodiments in the specification. *See* Op. Br. 14-15 (citing Ex. 1 ('912), p. 28, 12:66-13:25, 12:29-32).

Defendants are correct that there are two references to "use" in the Federal Circuit appellate brief. The first of these instances of "use" describes the claims, but does not state that all four signals must be "used," instead only referring to two of the four signals recited in the claims.

> Netlist was unambiguous that the logic element must "use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal[s]." Ex. Q at 28 (discussing only two of the four signals).

The second of these instances of "use" discusses what the specification discloses, not the claims: "the specification teaches . . . ." *Id.* at 34.

IV. The preambles of the '912 and '608 patent limit the claims to memory modules

The preamble of the '912 patent is limiting. For example, claim 15 recites a memory module that connects to "a computer system." The subsequent limitations then refer back to receiving signals from "the computer system": "a set of input signals from the computer system." The antecedent basis of "the computer system" is the preamble. If the memory module was not connected to the computer system's memory controller, it could not receive input signals. Defendants appear to have conceded the point of Netlist's proposal that the '912 patent claims should be limited to "memory modules" as distinct from other modular computer accessories. Resp. Br. 12.

For the '608 patent, Defendants clearly are reserving the right to attempt to read on other module computer devices, which would be contrary to the use of "memory module" in the '608 patent. '608, 1:55-57 ("A processor or a memory controller accesses the memory module via a memory bus"). Moreover, the preamble is required for antecedent basis. The preamble of claim 1 recites "a memory module operable to communicate with a memory controller via a memory bus" and then recites the

signal lines on this bus including "a set of control/address signal lines and a plurality of sets of data/strobe signal lines[.]" The limitations that follow the preamble recite "**the** memory bus," "**the** set of control/address signal lines," and "**the** plurality of sets of data strobe signals."

V. The "logic," "circuitry," and "data buffer control signals" terms

A. These terms do not require a "fork-in-the-road" approach.

Samsung does not argue that the specification in the issued patents requires a "fork-in-the-road" interpretation. Instead, it argues that because the term "control signals" were added through examiner's amendment in 2017 and 2019, those portions of the specification should be ignored. But whether the '215 and '417 patents are entitled to the 2004 priority date (they are) is a separate inquiry to how the terms should be interpreted in light of the specification. Under Federal Circuit case law, it is the specification as issued with the claims that constitutes the intrinsic record. *Sun Pharm. Indus., Ltd. v. Eli Lilly & Co.*, 611 F.3d 1381, 1388 (Fed. Cir. 2010) ("[P]recedent leaves no room for debate that the relevant specification for claim construction purposes is that of the issued patent . . . ."). The specifications as issued are replete with instances in which control signals are not used in a "fork in the road." *E.g.*, '215, Figs. 8A-8B, 12:44-59, 13:1-15.

Samsung ignores examples supporting a broader construction. For example, Netlist explained how Figures 8A and 8B of the '215 patent illustrate an embodiment without the "fork-in-the-road" arrangement. Op. Br. 20. Samsung attempts to dismiss these embodiments as "not relevant" because they relate to controlling data strobe signals (DQS) not data signals, Resp. Br. 18-19. Samsung is mistaken. The embodiments shown in Figures 8A and 8B include switches that isolate the DQS lines, but do ***not*** have switches that isolate the DQ lines of rank a and rank b which are both connected to the same common DQ data signal line. *See* Ex. 2 ('215), Figs. 8A, 8B. The lack of switches for the data lines is highlighted by comparing Figures 8A and 8B with Figures 8C and 8D, which include switches for both the DQ and DQS lines. *See* Ex. 2, Figs. 8C, 8D. Indeed, the specification clarifies that "[i]n

certain embodiments, the circuit 40 also provides the load isolation described above in reference to Figs. 1-5. For example, as schematically illustrated by Fig. 8C, the circuit 40 comprises both the switch 120 for the DQ data signal lines . . . and the switch 130 for the DQS data strobe signal lines . . . .” Ex. 2, 13:16-21. As that passage makes clear, the embodiments shown in Figures 8A and 8B are not such “certain embodiments,” and do not include the load isolation switches for the data signal lines. Accordingly, these embodiments support the plain language of the claims, which—again—include no limitations requiring the inventions to disable the data signal lines.

B. “circuitry” and “logic” are not subject to § 112, ¶ 6, and are not indefinite.

The “circuitry” and “logic” terms are not subject to 112, ¶ 6. *See* Op. Br. 21-23 (circuitry); *id.* at 15-17 (logic). The relevant claims here identify “circuitry” with sufficient qualifiers indicating structural meaning to a POSITA. *See id.* at 21-22; *Estech Sys., Inc. v. Target Corp.*, 2021 WL 1090747, at *23-24 (E.D. Tex. Mar. 21, 2021) (“circuitry for automatically calling [a] telephone extension” was not subject to § 112, ¶ 6 because the claim language included sufficient qualifying language). The relevant claims reciting the “logic” limitations also recite sufficient structure to a POSITA, such as “logic . . . providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer” in claim 1 of the ’215 patent and “logic . . . configurable to receive a set of input address and control signals . . . via the address and control signal lines” in claim 1 of the ’417 patent. *See Sonrai Memory Ltd. v. Oracle Corp.*, 2022 WL 800730, at *8-9 (W.D. Tex. Mar. 16, 2022) (Yeakel, J.) (distinguishing *Egenera, Inc. v. Cisco Sys.*, Inc., 972 F.3d 1367 (Fed. Cir. 2020)) and holding that the term “logic for directing transfer of data from said first memory array via said first bus to be processed by said compression/decompression logic and then transferred to said second memory array via said second bus” was not subject to § 112, ¶ 6). Even if subject to § 112, ¶ 6, neither term is indefinite because the specification discloses sufficient structure. *See* Op. Br. 23 (circuitry); *id.* at 17-18 (logic).

VI. "Burst of data strobe signals" is not indefinite

Micron fails to address precedent refuting its theory that a term is indefinite merely because it "is susceptible to differing interpretations." Op. Br. 25 (quoting *Nevro Corp. v. Boston Sci. Corp.*, 955 F.3d 35, 41 (Fed. Cir. 2020)). Unlike the two cases Micron cites addressing failures to distinguish between multiple ways to measure a claimed property, Resp. Br. 24, the '215 patent makes clear that the claims cover ***both*** combined and non-combined strobe signals. *See* Op. Br. 26.

VII. "operable in a computer system to communicate data"

Defendants rely solely on the inapposite *TQ Delta* case. Resp. Br. 20. In that case, this Court differentiated claims reciting both "operable to" and "configurable to." *TQ Delta, LLC v. CommScope Holding Co.*, 2022 WL 2071073 (E.D. Tex. June 8, 2022). Here the patentee chose to distinguish between "operable" and "configured to." Op. Br. 26-28.

VIII. The plain and ordinary meaning of the "CAS latency" terms is not indefinite

Micron's constructions should be rejected because they are unmoored from the claims (which encompass read/write commands), the specification, and the JEDEC standards. Op. Br. 29-30. Micron contends that the "wherein" clause of '417 claim 1 is indefinite. Resp. Br. 21. Micron is incorrect. Under Micron's construction, the claim is allegedly indefinite because "the claim recites read and write commands." But this just counsels against limiting the "CAS latency" terms to read commands. *Omega Eng'g, Inc., v. Raytek Corp.*, 334 F.3d 1314, 1335 n.6 (Fed. Cir. 2003) ("[T]he district court's claim construction inevitably required the invalidation of claims 33 and 41, in contradiction to the canon that courts should attempt to construe claims to preserve their validity. . . . Since the intrinsic evidence did not compel the invalidating construction, the district court thus erred."). As to Netlist's construction, Micron does not contend that the plain meaning of these terms is indefinite, but rather, cites to Netlist's "alternative" constructions in a case involving a different patent. Ex. 37 at 8-9. Netlist did not propose those constructions here, so Micron's concern is moot. *See* Dkt. 94-1 at 115-116, 119.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing document was served on Samsung's counsel through the Court's CM/ECF system on September 14, 2023.

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